R09

Code No: D109115704

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.Tech I Semester Regular Examinations March 2010
ALGORITHMS FOR VLSI DESIGN AUTOMATION
(COMMON TO EMBEDDED SYSTEMS & VLSI DESIGN, VLSI & EMBEDDED SYSTEMS, VLSI SYSTEM DESIGN / VLSI DESIGN /VLSI)

Time: 3hours **Max.Marks:60**

Answer any five questions
All questions carry equal marks

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1.a) Explain about the most important entities in VLSI Design.
b) How are the actions involved to design VLSI circuit to be grouped? Explain about Design Actions.

2.a) Explain about the unit-size placement problem.
b) What are the two methods for finding the optimal solution of a combinatorial optimization problem? Explain.

3.a) Give a Pseudo-code description of Tabu search and explain the same.
b) Give an example for a genetic algorithm and explain the same.

4.a) Explain about Allocation, Assignment and Scheduling of Algorithms in high-level synthesis.
b) Explain about optimization issues in High-level synthesis.

5. With an example explain how high level transformations can be carried out on Data Flow Graphs. What are the advantages and limitations?

6.a) Explain about various FPGA Technologies with necessary diagrams.
b) What are the various steps in the physical Design cycle of FPGA's? Explain.

7.a) How Multichip Modules are classified? Explain about MCM physical Design cycle.
b) How MCM portioning is carried out? Explain with the help of a system graph.

8. Write notes on any TWO:
i) Pin distribution and routing in MCM's.
ii) Binary-Decision Diagrams.
iii) Integer Linear Programs.

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